REMARKS

Claims 1-4, 6-11, 14-17 and 33-34 are pending. Claim 12 has been cancelled. Claims 1, 10, 15 and 33 have been amended. Reconsideration and allowance of the pending claims is respectfully requested.

Claim Objections

Claim 10 has been amended as requested and claim 12 has been cancelled, thereby obviating the objections. Withdrawal of the objections is respectfully requested.

Claim Rejections § 103(a)

Claims 1, 3, 4, 6-10, 12, 14-16, 33 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent Number 6,118,181 to Merchant et al (hereinafter "Merchant") in view of United States Patent Number 5,702,962 to Terasawa (hereinafter "Terasawa"). Claims 2, 11 and 17 were rejected under 36 U.S.C. § 103(a) as being unpatentable over Merchant and Terasawa and further in view of United Stated Patent Number 5,668,033 to Ohara et al. (hereinafter "Ohara"). The Applicant has amended Claims 1, 10, 15 and 33, which will be described in greater detail after discussion of the references.

The References

Merchant describes a system and method for bonding wafer. Although Merchant describes integrated circuits on two wafers, Merchant recites that "most conventional wafer bonding processes are not suitable for bonding wafers that include CMOS circuitry and other temperature sensitive components because the relatively high temperatures associated with the

bonding process can damage the CMOS circuitry or other temperature sensitive components." *See Merchant, Col. 1, Lines 34-39.* Merchant then describes an instance of such an undesirable and unacceptable bonding technique in the following excerpted portion:

> In addition, it is often undesirable to use eutectic bonding in order to bond two wafers together because the existence of liquid phases in these processes can sometimes lead to rapid dissolution of underlayers and, hence, a loss of process control. Furthermore, maintaining precise separation distances between two wafers bonded via eutectic bonding can be difficult since the surfaces of the eutectics typically deform when a temperature close to the eutectic's melting point is reached. *Merchant, Col. 1, Lines 52-62.*

Consequently, Merchant describes a bonding process that uses palladium in response to the undesirability of eutectic bonding. Merchant also cautions that "one skilled in the art should realize that substituting for the silicon and/or palladium may affect the temperatures associated with the bonding process". *See Merchant, Col 6, Lines 24-23 and 17-19.* Therefore, Merchant explicitly cautions against the use of materials other than palladium and against the use of eutectic bonding.

Further, Merchant describes the following:

> It should be further noted that the adhesion of palladium to chromium has been found to depend directly on the cleanliness of the chromium layer 29 surface. Therefore, it is preferable to perform a brief (i.e., approximately 1 to 2 minutes) 150 W rf sputter-etch cleaning of the chromium layer 29 surface just prior to application of the palladium layer 27 to the chromium layer 29. *Merchant, Col. 4, Lines 31-37.*

Thus, Merchant discloses sputter-etch cleaning of the chromium layer before adhesion of the palladium. Nowhere does Merchant disclose, teach or suggest a bond structure having an alloy that is sufficient to remove a native oxide.

Terasawa describes a fabrication process for a static induction transistor. In the fabrication process of Terasawa, an oxide film is removed with hydrofluoric acid, as shown in the following excerpt:

> The naturally formed oxide film is then removed with hydrofluoric acid as needed, and the N.sup.- substrate 10 and the N.sup.+ substrate 20 are subjected to ultrasonic cleaning with purified water and dried by a spin dryer at room temperature *Terasawa, Col. 4, Lines 47-50.*

To clean the surfaces, Terasawa describes the following:

> The N.sup.- substrate 10 and the N.sup.+ substrate 20 are then subjected to ultrasonic cleaning with an aqueous solution of sulfuric acid and hydrogen peroxide, thereby removing organic substances and metals on the substrates. *Terasawa, Col. 9, Lines 13-16.*

Thus, Terasawa discloses the use of acids to remove oxide films and clean surfaces. Nowhere does Terasawa disclose, teach or suggest a bond structure having an alloy that is sufficient to remove a native oxide.

Ohara describes a method for manufacturing a semiconductor acceleration sensor device by "covering a movable portion by use of a cap". *See Ohara, Col. 1, Lines 51-52.* Ohara describes the bonding of the cap as follows:

> Also, preferably, a gold (Au) film is adhered to the leg portion of the cap forming wafer. Where the bonding frame is made to be formed using silicon (Si), when in the bonding step heating is performed up to a temperature higher than an Au/Si eutectic temperature, the gold film comes to function as a bonding layer, with the result that it is possible to obtain a tough bondage easily. Further, when the gold film is also adhered onto the inner surface of the cap, the gold film can be also made to function as an electromagnetic shielding layer. *Ohara, Col. 2, Lines 23-32.*

Thus, Ohara merely describes a cap which is bonded using a gold film. The cap described in Ohara merely serves to protect the movable portion of the semiconductor acceleration sensor. The gold film is utilized as a bond via a eutectic technique and may function as an electromagnetic shield. Nowhere does Ohara disclose, teach or suggest an integrated circuit in the cap.

<u>**The Claims**</u>

Claim 1 has been amended, and as amended (portions of the amendment appear in bold italics below) recites an electrical device comprising "first and second substrates having respective first and second integrated circuits" and "a bond structure ... composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed ***such that the alloy is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate*** ... [and] configured to form an electrical connection between the first integrated circuit and the second integrated circuit". Support for the amendment may be found throughout the specification and drawings as filed, such as at page 7, paragraph 25 of the subject application. Neither Merchant nor Terasawa, alone or in combination, disclose, teach or suggest the above excerpted limitations as claimed in amended Claim 1.

Claim 10 has been amended, and as amended (portions of the amendment appear in bold italics below) recites an electrical device comprising "first and second semiconductor wafers each including a plurality of integrated circuits", "the silicon layer on the first semiconductor wafer is bonded to the second semiconductor wafer by gold alloyed with an oxide affinity material than that of silicon ***such that the gold alloyed with the oxide affinity material is sufficient to remove a native oxide from the first semiconductor wafer***",

and "the gold alloyed with the oxide is configured to provide an electrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer". Support for the amendment may be found throughout the specification and drawings as filed, such as at page 7, paragraph 25 of the subject application. Neither Merchant nor Terasawa, alone or in combination, disclose, teach or suggest the above excerpted limitations as claimed in amended Claim 10.

Claim 15 has been amended, and as amended (portions of the amendment appear in bold italics below) recites an electrical device comprising "first and second semiconductor wafers each including a plurality of integrated circuits", and "the first semiconductor wafer is bonded to the second semiconductor wafer by the gold alloy that is bonded to the silicon on the first semiconductor wafer such that the gold alloy is configured to ***remove a native oxide from the silicon; and*** provide an electrical connection between at least one said integrated circuit of the first semiconductor wafer with at least one said integrated circuit of the second semiconductor wafer". Support for the amendment may be found throughout the specification and drawings as filed, such as at page 7, paragraph 25 of the subject application. Neither Merchant nor Terasawa, alone or in combination, disclose, teach or suggest the above excerpted limitations as claimed in amended Claim 15.

Claim 33 has been amended, and as amended (portions of the amendment appear in bold italics below) recites an electrical device comprising "first and second substrates bonded together with a first material having dispersed therein a reducing agent for the diffusion therein of oxidation of a second material" and "the first material having the dispersed reducing agent is configured to: ***remove a native oxide from the first substrate or the second***

substrate; and form an electrical connection between a first integrated circuit on the first substrate with a second integrated circuit on the second substrate". Support for the amendment may be found throughout the specification and drawings as filed, such as at page 7, paragraph 25 of the subject application. Neither Merchant nor Terasawa, alone or in combination, disclose, teach or suggest the above excerpted limitations as claimed in amended Claim 33.

As previously described, Merchant describes a system for bonding wafers that involves "sputter-etch cleaning of the chromium layer 29 surface just prior to application of the palladium layer 27 to the chromium layer 29". *Merchant, Col. 4, Lines 35-37.* Terasawa describes a fabrication process for a static induction transistor that involves removal of an oxide film with hydrofluoric acid. *See Terasawa, Col. 4, Lines 47-50.* Neither Merchant nor Terasawa, alone or in combination, disclose, teach or suggest a bond structure composed of an "alloy [that] is sufficient to remove a native oxide from an interface surface between the bond structure and the first substrate" as claimed in Claim 1, nor a bond formed by "gold alloyed with the oxide affinity material [that] is sufficient to remove a native oxide from the first semiconductor wafer" as claimed in Claim 10, nor a "gold alloy [that] is configured to remove a native oxide from the silicon" as claimed in Claim 15, nor "first and second substrates bonded together with a first material ... having the dispersed reducing agent [that] is configured to: remove a native oxide from the first substrate or the second substrate" as claimed in Claim 33. Ohara does not correct these defects.

As previously described, Ohara describes a method for manufacturing a semiconductor acceleration sensor device by "covering a movable portion by use of a cap". *See Ohara, Col. 1, Lines 51-52.* The cap described in Ohara merely serves to protect the movable portion of the semiconductor acceleration

sensor. The gold film is utilized as a bond via a eutectic technique and may function as an electromagnetic shield. Nowhere does Ohara disclose, teach or suggest an integrated circuit in the cap and therefore cannot disclose, teach or suggest using the bond to communicatively couple integrated circuits on each of the wafers. Indeed, the Office correctly asserts that Ohara does not "explicitly disclos[e] the plurality of integrated circuit[s] on each [of the] wafers". *See Office Action Dated April 28, 2004, Page 5.*

Merchant, however, describes that it is often undesirable to use eutectic bonding techniques, as shown in the following excerpted portion:

> In addition, it is often undesirable to use eutectic bonding in order to bond two wafers together because the existence of liquid phases in these processes can sometimes lead to rapid dissolution of underlayers and, hence, a loss of process control. Furthermore, maintaining precise separation distances between two wafers bonded via eutectic bonding can be difficult since the surfaces of the eutectics typically deform when a temperature close to the eutectic's melting point is reached. *Merchant, Col. 1, Lines 52-62.*

Consequently, Merchant describes a bonding process that uses palladium in response to the undesirability of eutectic bonding. Merchant also cautions that "one skilled in the art should realize that substituting for the silicon and/or palladium may affect the temperatures associated with the bonding process". *See Merchant, Col 6, Lines 24-23 and 17-19.* Because Merchant explicitly cautions against the use of materials other than palladium and against the use of eutectic bonding as described by Ohara, the combination of Merchant, Ohara and Terasawa would not result in an electrical device having the above-listed claim limitations of Claims 1, 10, 15 and 33. For instance, the eutectic bonding techniques of Merchant for attaching a cap would not result in first and second substrates, each having integrated circuits that are communicatively coupled

via the bond because Merchant cautions against the use of eutectic techniques when attaching two substrates having integrated circuits. Thus, a combination of the gold bonded cap of Ohara with the palladium bond of Merchant and the transistor of Terasawa would not result in the claimed limitations as described above.

Further, there is not motivation for the asserted combination contained in the references. Neither Merchant nor Terasawa disclose, teach or suggest any deficiencies with the recited techniques used to clean and remove oxides. Ohara does not teach or suggest that the described bond is suitable for providing an electrical connection between integrated circuits. Therefore, a person of ordinary skill in the art, when viewing Merchant and Terasawa, would not be motivated to look to Ohara for a bonding technique that is utilized to attach a cap. Accordingly, it is respectfully submitted that Claims 1, 10, 15 and 33 are allowable over Merchant, Terasawa, and Ohara, alone and in combination. Withdrawal of the rejections is respectfully requested.

Claims 2-4 and **6-9** depend from independent Claim 1. **Claims 11** and **14** depend from independent Claim 10. **Claims 16-17** depend from independent Claim 15. **Claim 34** depends from independent Claim 33. Each of these claims is allowable based on their respective dependencies as well as their own recited features which are not disclosed, taught, or suggested by Merchant, Terasawa or Ohara, alone or in combination.

Conclusion

For at least these reasons, Claims 1-4, 6-11, 14-17 and 33-34 are allowable and furtherance to issuance is respectfully requested.

Respectfully submitted,

Dated: 11/16/04

By: [signature]
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